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4/26/06

**IN THE SPECIFICATION:**

Please replace the third and fourth full paragraphs of specification page 2 with the following replacement paragraphs:

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FIG. 3 shows a complete bidirectional system using the serializers as in FIG. 1 and ~~deserializer~~deserializers as in FIG. 2. Note that there are eight data lines and a single clock into each serializer and out from each ~~deserializer~~deserializer. The data and clock lines between the serializer and the ~~deserializer~~deserializer are typically differential signals each using two conductors.

The serializer/deserializer~~deserializers~~ of FIG. 3 each contain a PLL that are common in such devices, but PLL's consume significant power, are complex, require long locking times, and occupy considerable chip real estate. It would be advantageous to dispense with PLL's.

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Please replace the third full paragraph of specification page 5 with the following replacement paragraph:

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In view of the foregoing background discussion of the prior art, the present invention provides advantages in serializer/deserializer~~deserializer~~ and a method for sending and receiving serial data without using phase of delay locked loops. The serializer/deserializer~~deserializer~~ sends out a data word bit by bit and receives a data word bit